Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.257”**

**.257”**

**SOURCE**

**GATE**

**BACKSIDE IS DRAIN**

**Top Material: Al**

**Backside Material: Cr/Ni/Si**

**Bond Pad Size: S = .051 x .069”**

**G = .018 x .026”**

**Backside Potential: Drain**

**Maske Ref: D27**

**APPROVED BY: DK DIE SIZE .257” X .257” DATE: 7/11/22**

**MFG: HARRIS THICKNESS .014” P/N: IRFC250**

**DG 10.1.2**

#### Rev B, 7/19/02